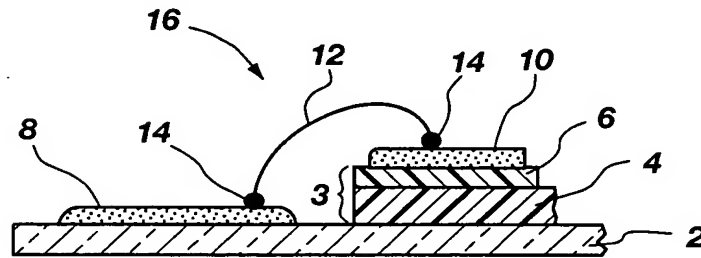
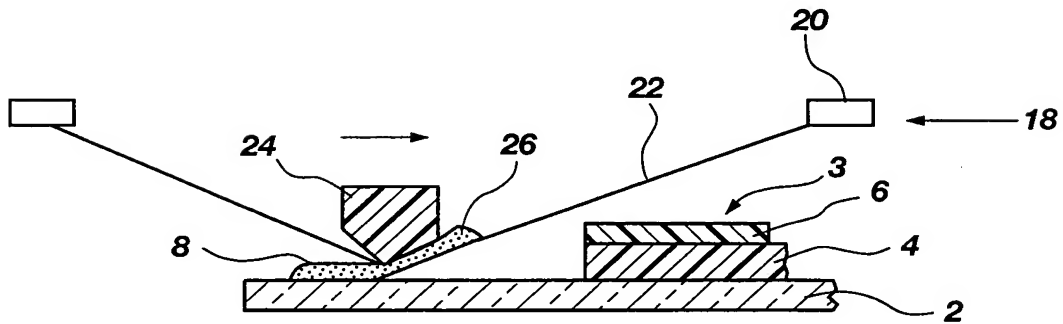


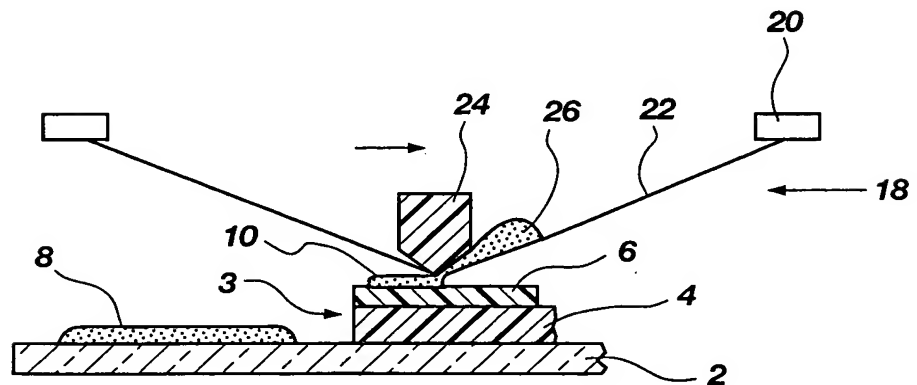
1/8



**Fig. 1A**  
**(PRIOR ART)**

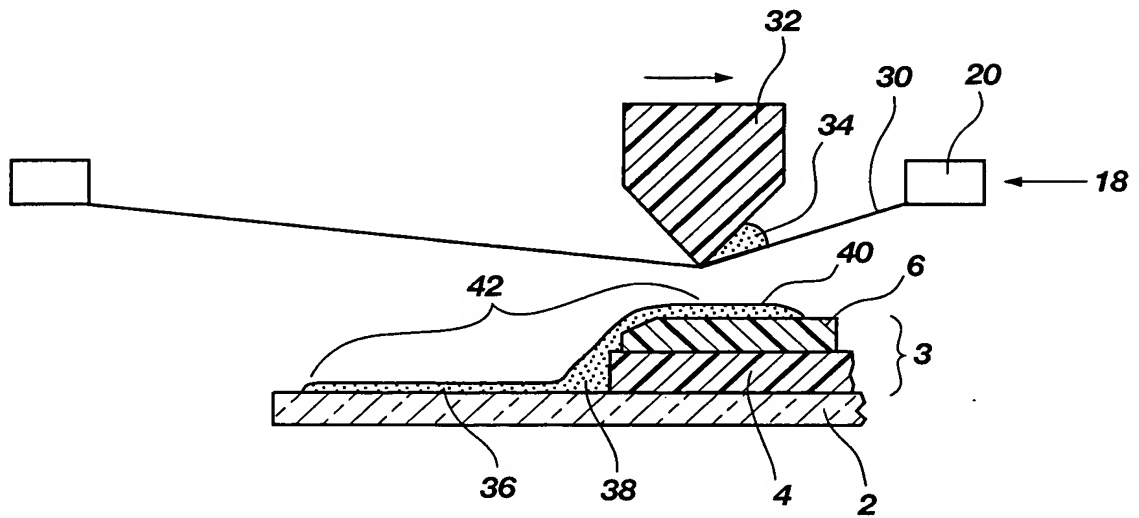


**Fig. 1B**  
**(PRIOR ART)**



**Fig. 1C**  
**(PRIOR ART)**

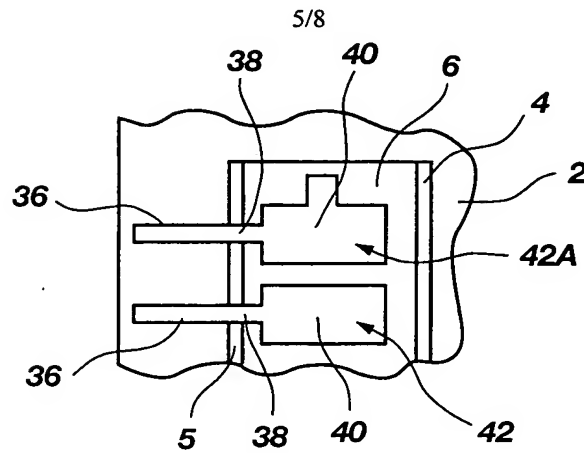




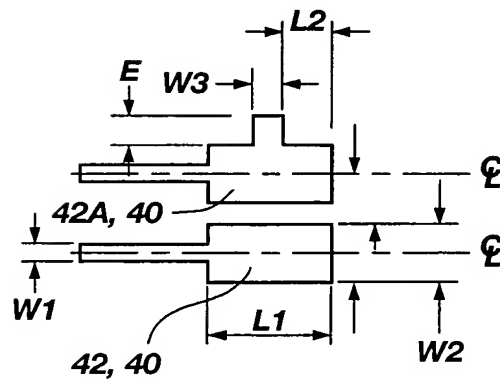
**Fig. 2D**

FIG. 7 is a schematic diagram showing a top-down view of a device assembly. The assembly includes a central rectangular area (3) surrounded by a frame (6). On the left side, there is a vertical array of components (42A, 42B) connected to a bus or interface (3C). Arrows indicate directions 3B and 44.

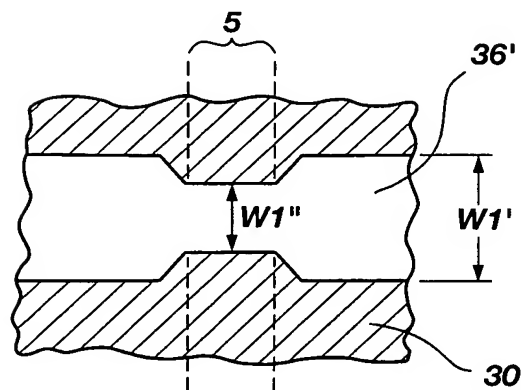
**Fig. 3A**



**Fig. 3C**



**Fig. 3D**



**Fig. 3E**

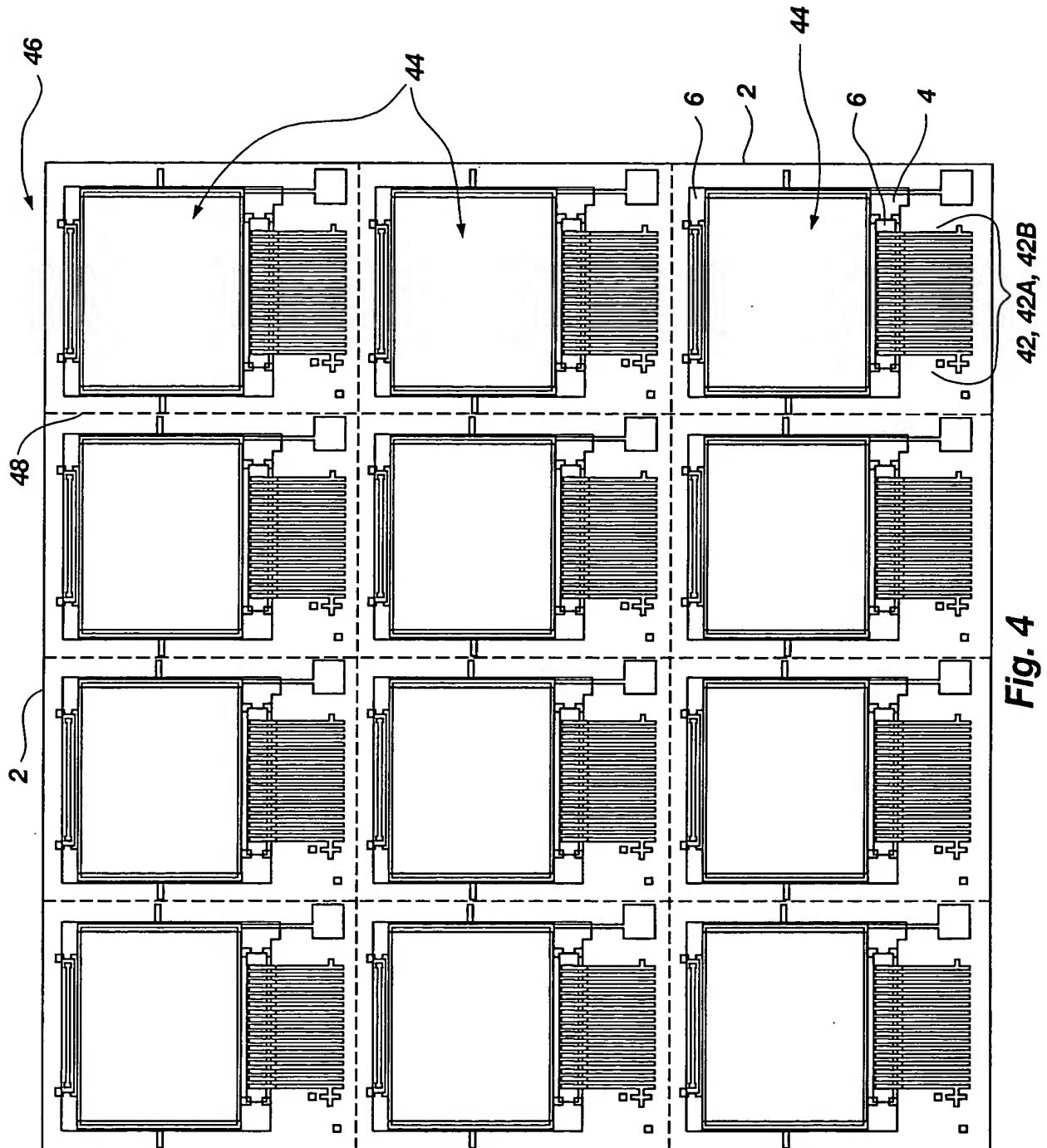
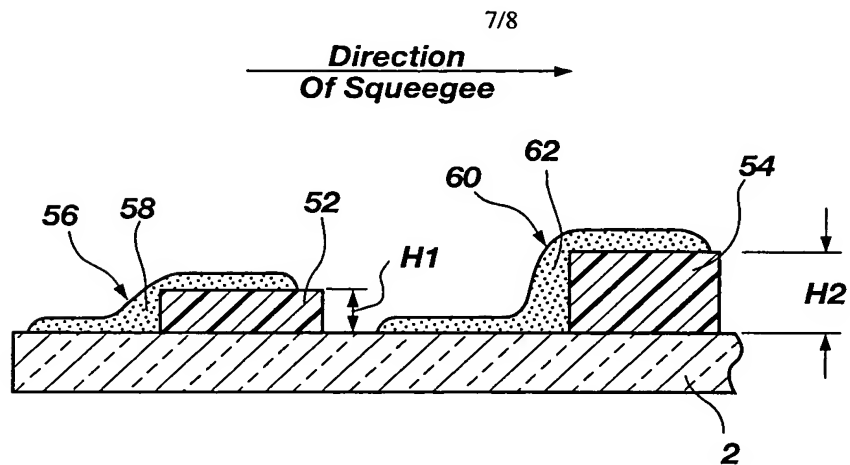
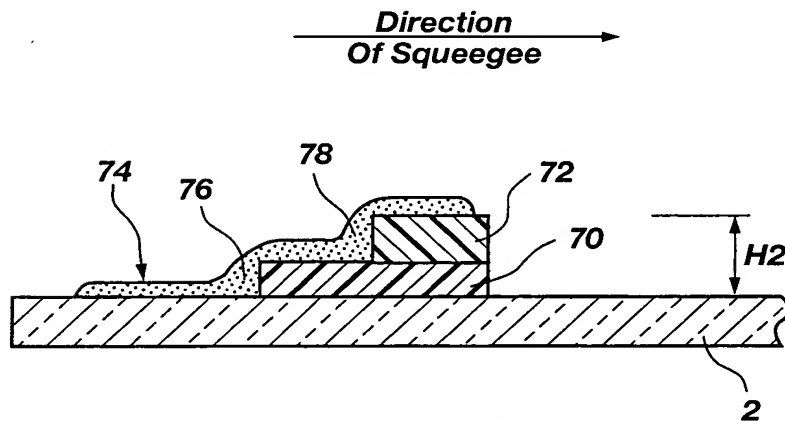


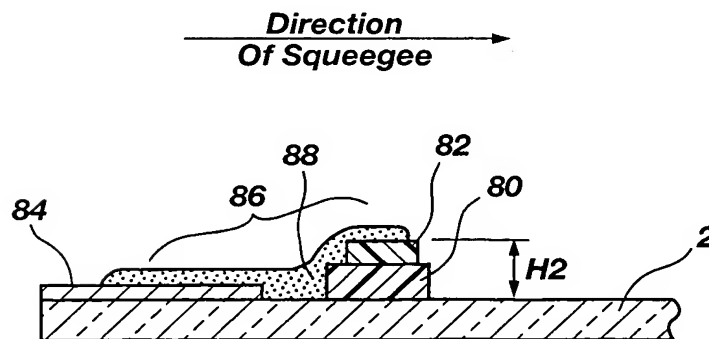
Fig. 4



**Fig. 5**



**Fig. 6**



**Fig. 7**

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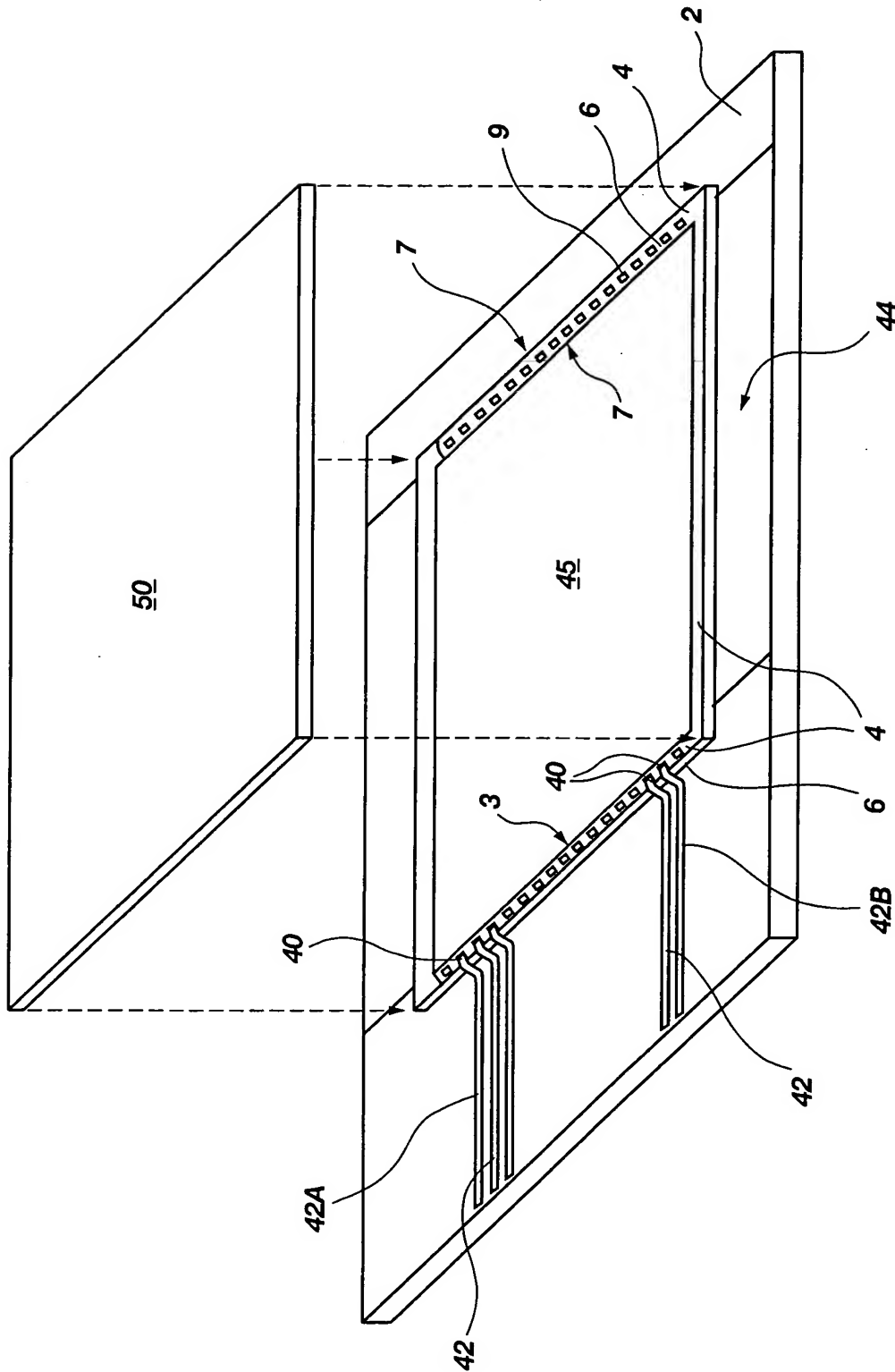


Fig. 8